NOvA Electronics/DAQ

Leon Mualem

University of Minnesota
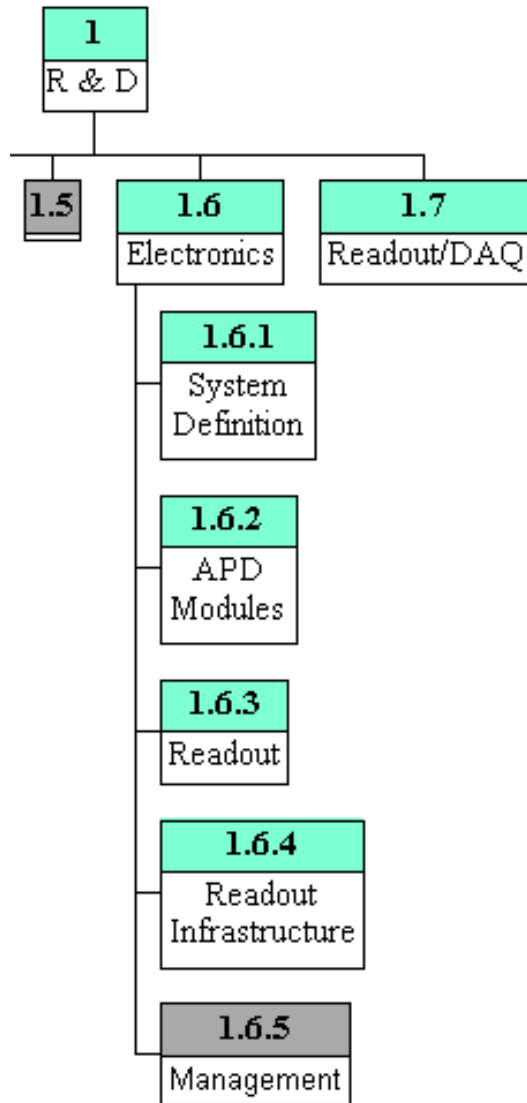
Outline

- Electronics WBS structure

- Recent work in Electronics

- DAQ WBS structure
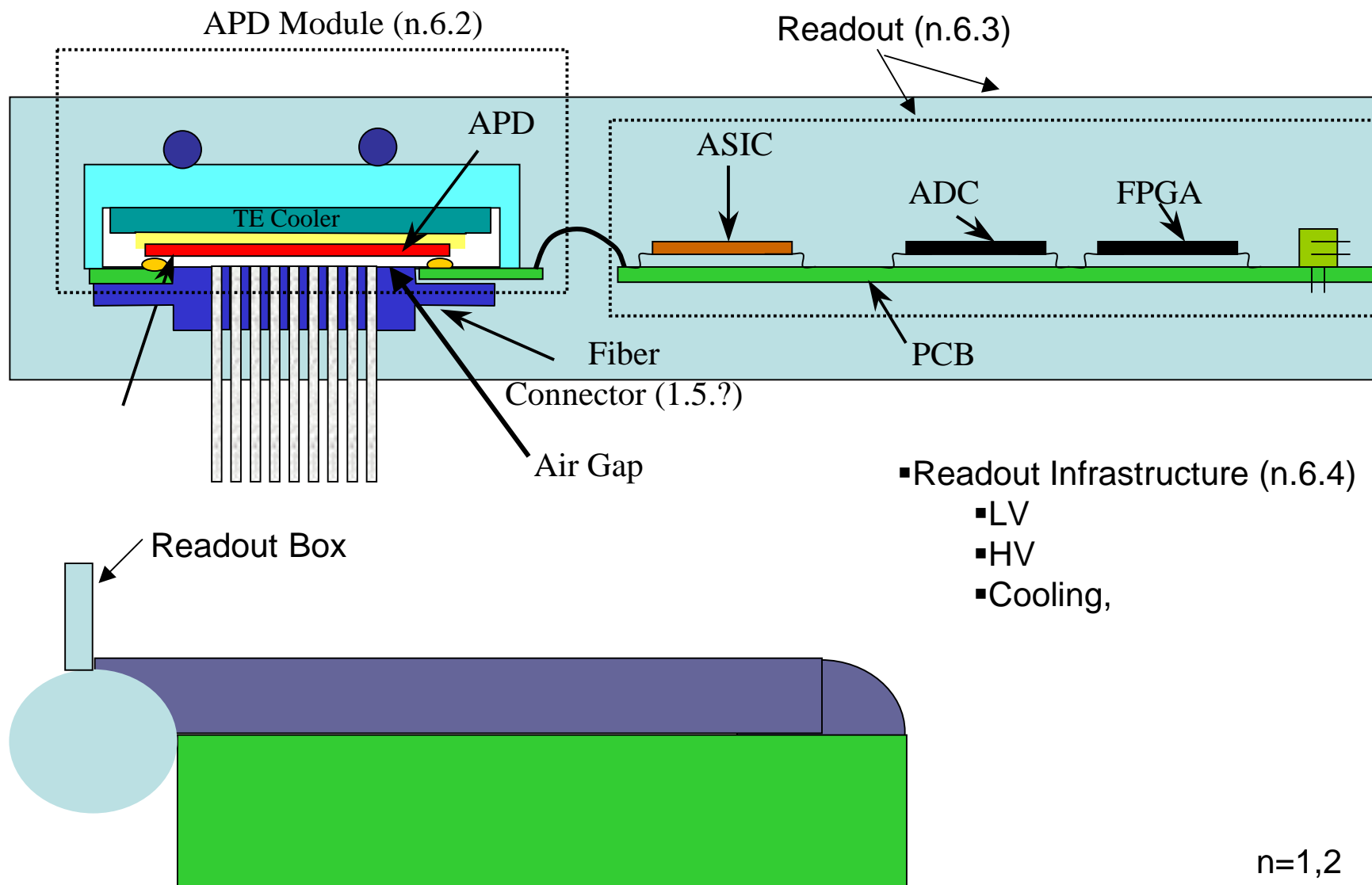
- Recent work in DAQ

- Open tasks

Electronics Organization

- **Documentation task**

- **Major Subsystems**
  - APD Modules
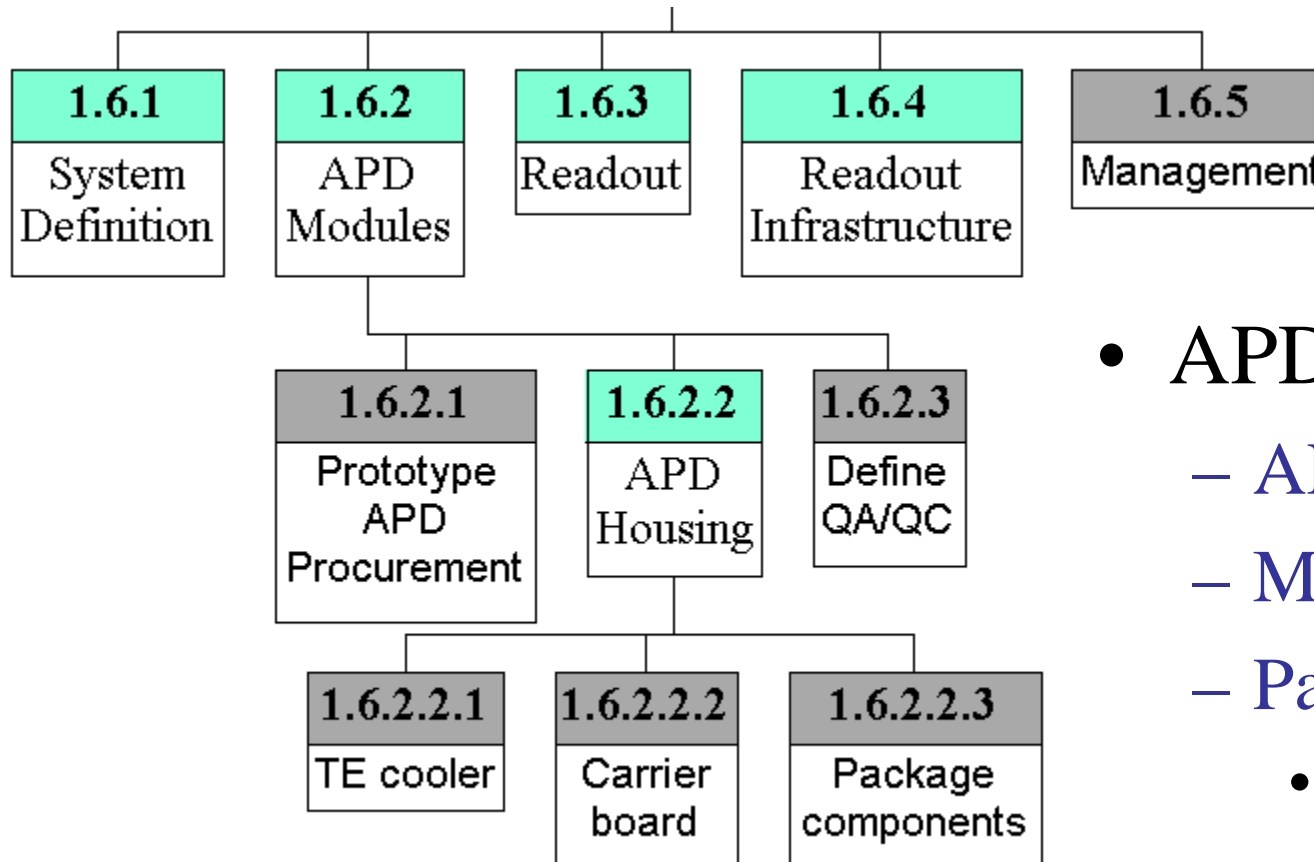 - Readout Modules
  - Readout Infrastructure

Electronics Concept

APD Module (n.6.2)

Readout (n.6.3)

APD

ASIC

ADC

FPGA

TE Cooler

Fiber

Connector (1.5.?)

PCB

Air Gap

▪Readout Infrastructure (n.6.4)
  ▪LV
  ▪HV
  ▪Cooling,

Readout Box

n=1,2

APD Modules

- **APD Module Task**
  - APD
  - Mounting
  - Packaging
    - Alignment
    - Isolation
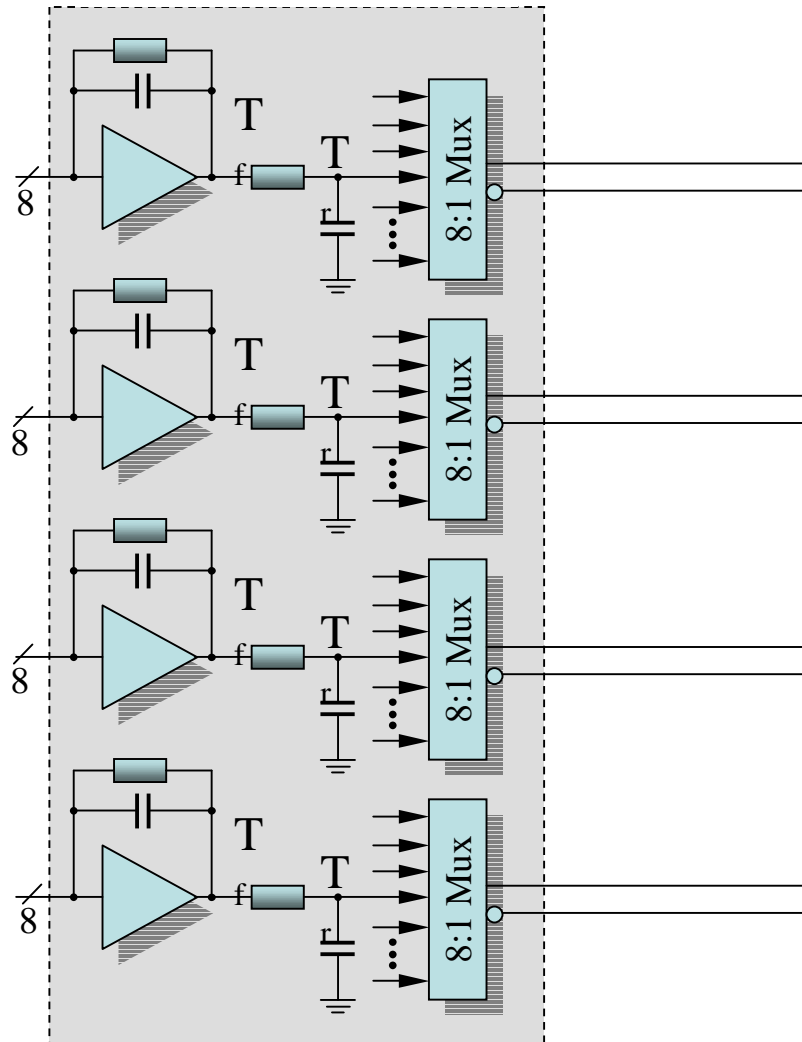
Front-End Readout options.

- Two options have been considered for the design of the front-end readout the APD.
- Continuous Digitization
  - 100% live
  - Allows for SuperNOvA triggers
  - Decouples spill trigger delivery
- Pipelined
  - No Digital Activity during acquire—quiet
- Prototype chip will do BOTH
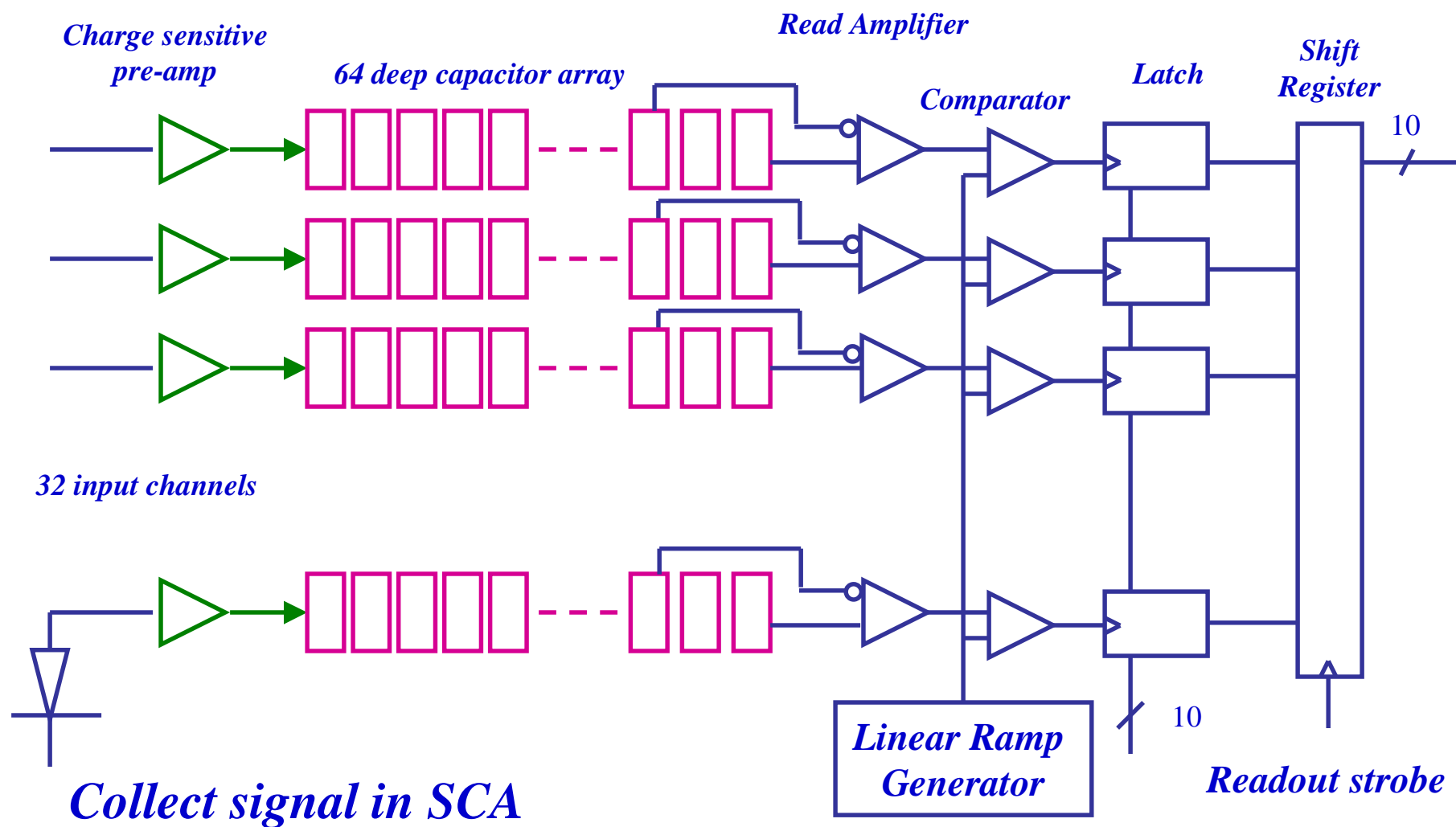
Continuous Digitization

32 channel front end ASIC

- (4x) 8:1 Analog multiplexers
- Each runs at 16 MHz
- 62.5 ns settling time per channel
- 500 ns equivalent sampling time

# SCA

Charge sensitive pre-amp

Read Amplifier

64 deep capacitor array

Comparator

Latch

Shift Register

10

32 input channels

Collect signal in SCA

Linear Ramp Generator

10

Readout strobe

Digitize Later

NOvA Electronics and DAQ

8

Fast Digitization Mode.

- Variants on the standard operation are included in the design.
  - Direct in to latch.
  - Non-linear ramp.
  - Complete digitization in 400 nsec.

Read Amplifier

Comparator
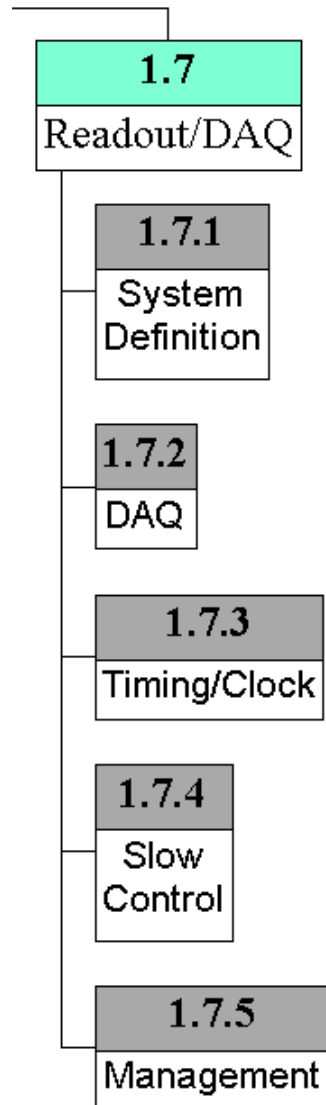
Latch

Non-linear ramp
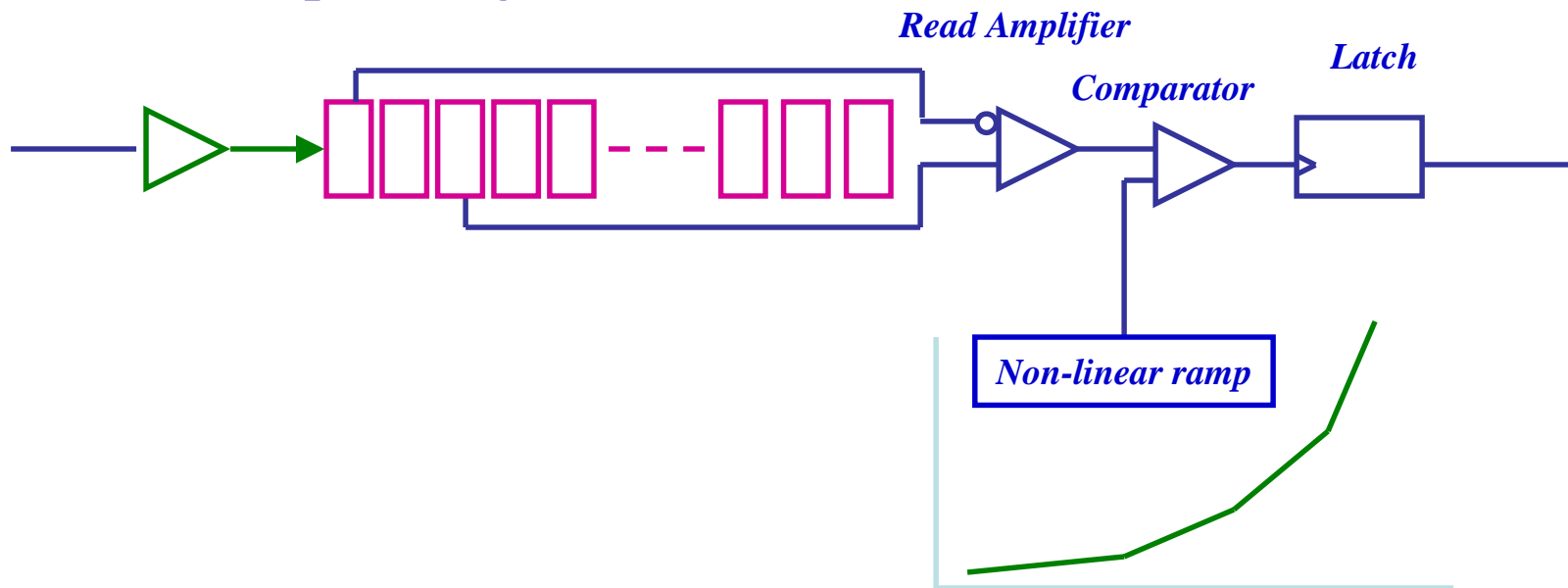
Front-End ASIC Status

- Design complete.
- Full simulations complete. Calculated noise level with 10 pf and 250 nsec shaping is 150 electrons. Reality: expect ~200.
- Layout of one SCA channel complete
- Layout of Control and MUX readout started
- Plan is to submit chip combining all readout options for November MPW run.

DAQ Organization

1.7
Readout/DAQ

1.7.1
System Definition

1.7.2
DAQ

1.7.3
Timing/Clock

1.7.4
Slow Control

1.7.5
Management

- Documentation task
- Major Subsystems
  - DAQ/Readout
    - Readout Box -> Enstore
  - Timing/Clock/Spill
    - Sync 500ns digitization clocks
    - Produce/Receive Spill times
  - Slow Control
    - Run control
    - State information, HV, cooling, …

Issues for DAQ

- Large number of isolated independent elements –23808 modules with APD boxes
  - Modules don't have enough information to determine interesting events
  - Large background of uninteresting events
    - 99.9% of events are "spare" muons not needed for calibration
- Physically large detector 16m x 16m x 132m
- Remote location –Spill trigger communication

Recent Work in DAQ

- 5-24-2005 Addition of several enthusiastic former BTeV collaborators ~~augments~~ creates "NOvA DAQ group"
  - Mark Bowden, Jerry Guglielmo, Vince Pavlicek, Margaret Votava, …

- 7-15-2005 Created a DAQ conceptual design for preliminary director's review

Data Rates

- Driven by cosmic muons, ~250kHz, leading to ~400Hz/channel or 12kHz/module rate
  - 120kB/module/s
  - But 23,808*120kB/s=~3GB/s

Buffering Requirements

- Asynchronous spill trigger requires only 1-2 seconds of buffering

- Buffering driven by Supernova Triggering requiring up to 20 seconds of buffer

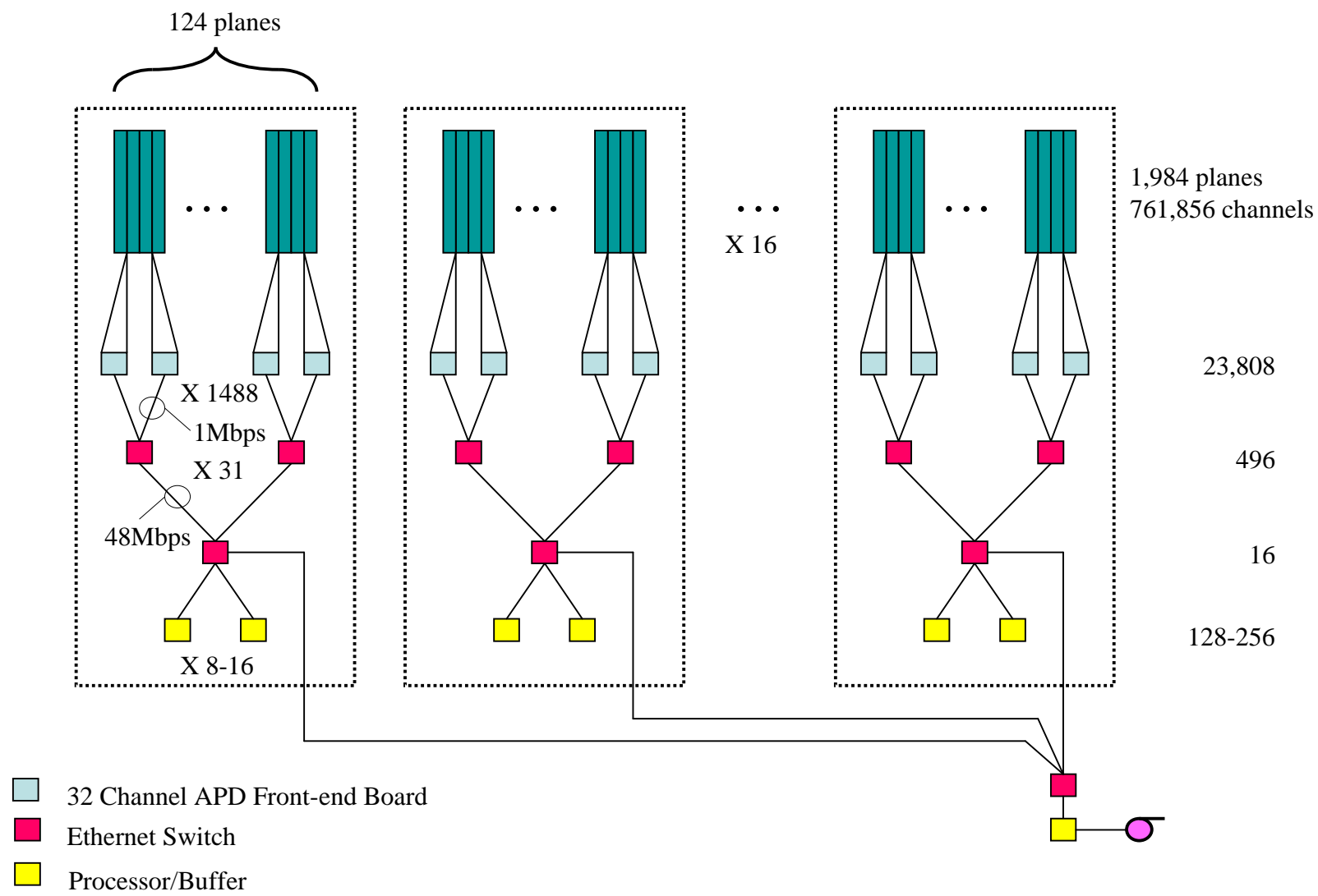 – Most significant signal comes early, so maybe less would be okay

A DAQ Plan

- Subdivide detector into segments
  - 16, 8 each in X and Y
  - Distributes buffering and triggering
  - Each is roughly a giant 16m cube with relatively few muons going between cubes
  - Do simple track finding in cubes to eliminate muon hits
  - Tally number of coincidences from remainder
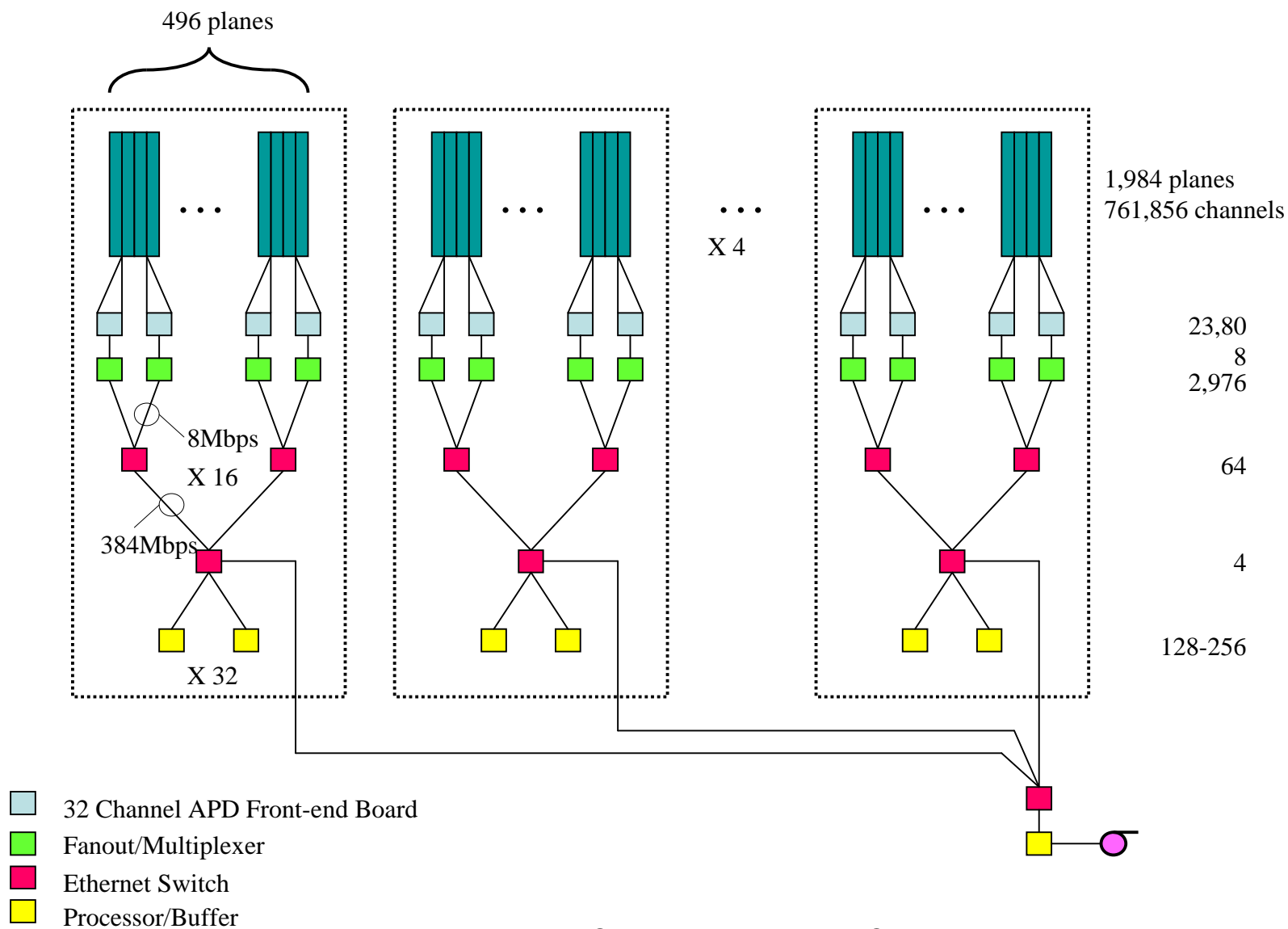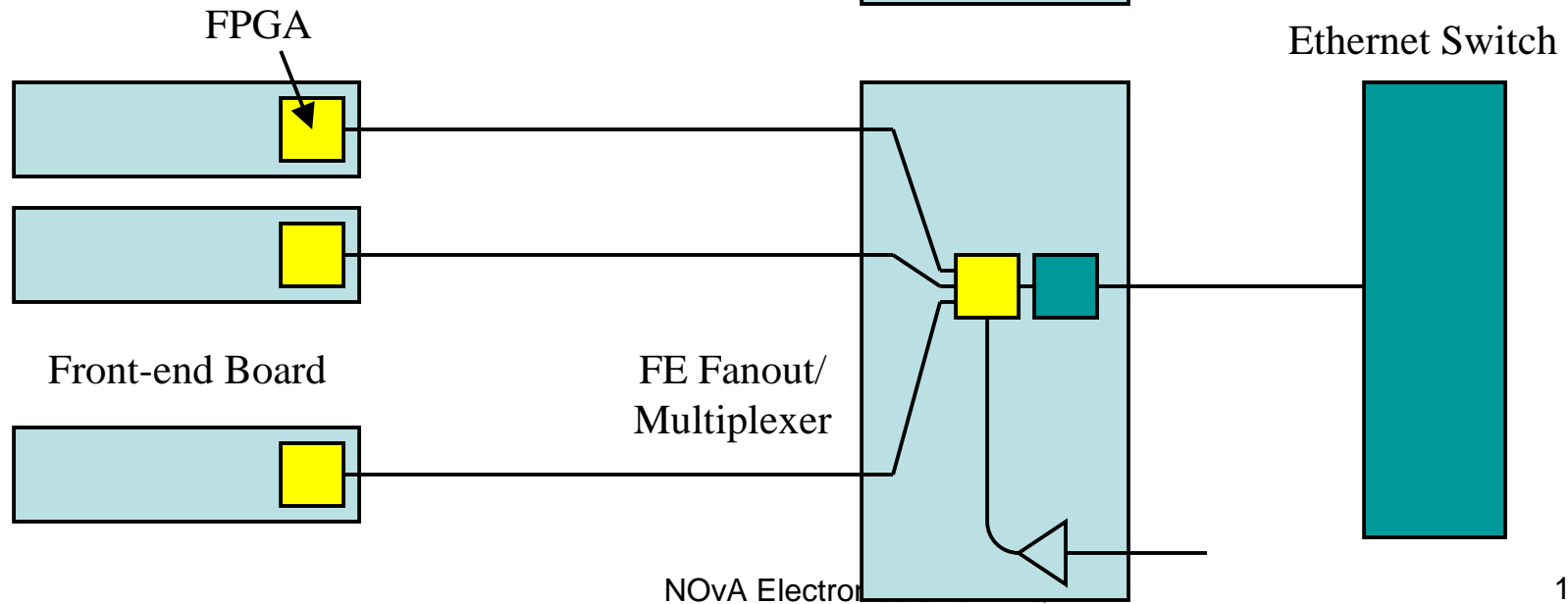 - Trigger if threshold met, or timing (in-spill or random) is satisfied
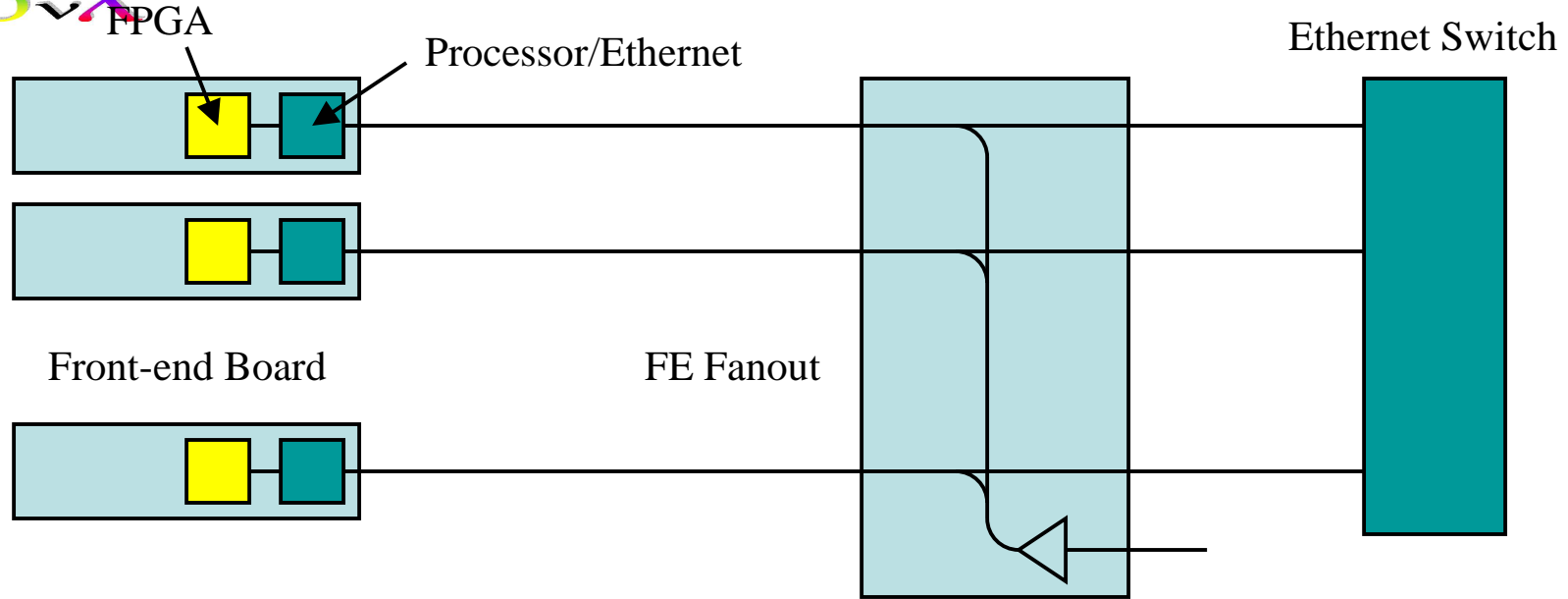
DAQ Diagram

124 planes

1,984 planes
761,856 channels

X 16

23,808

X 1488

1Mbps

X 31

496

48Mbps

16

X 8-16

128-256

32 Channel APD Front-end Board

Ethernet Switch

Processor/Buffer

A Plan B

496 planes

1,984 planes
761,856 channels

X 4

23,80
8
2,976

8Mbps

X 16

64

384Mbps

4

X 32

128-256

□ 32 Channel APD Front-end Board
■ Fanout/Multiplexer
■ Ethernet Switch
■ Processor/Buffer

Front-end Interface

FPGA

Processor/Ethernet

Ethernet Switch

Front-end Board

FE Fanout

FPGA

Ethernet Switch

Front-end Board

FE Fanout/
Multiplexer

NOvA Electro...

Network Buffering Options
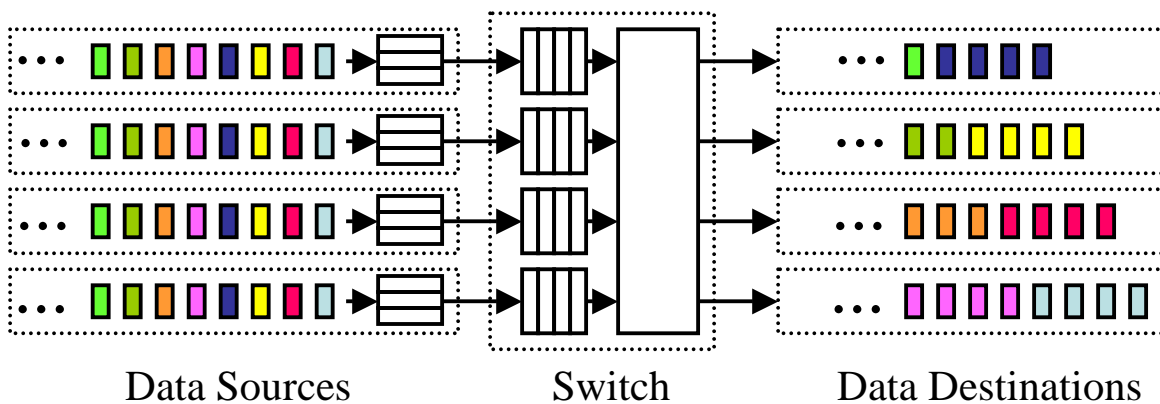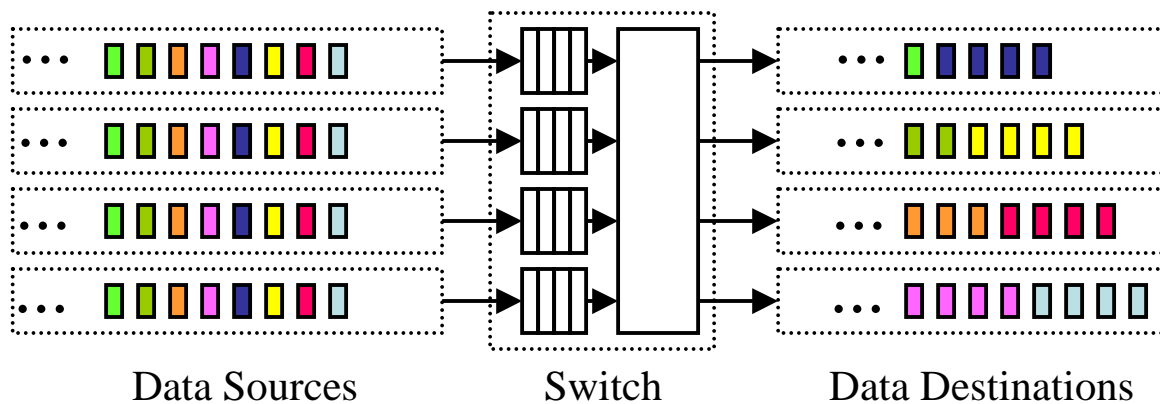

Data Sources   Switch   Data Destinations

Data Sources   Switch   Data Destinations

DAQ Parameters

- Buffering locations
  - Front end, switch, fan-in
- Time Slicing
- Segmentation
- Optimize Available Bandwidth

- Lots of knobs, lots of decisions

Open Electronics Tasks

- ## Readout Infrastructure
  - ### Low Voltage
    - 5W*25,000=125kW
    - 25kW quiet, 100kW not so quiet
    - Reliable
  - ### HighVoltage
    - 400V*1nA*800,000=0.32W, very quiet
    - Reliable
  - ### Cooling
    - Heat sinking 125kW
    - Reliable

Open DAQ Tasks

- DAQ
  - Optimizing time slice, segmentation
    - Efforts at FNAL
  - Supernova Triggering
    - Efforts begun at Harvard
- Timing/Clock/Spill
  - Synchronize digitization
  - Synchronize clocks
  - Send spill times
- Slow Control
  - Run Control
  - HV, Temp setting/readback
  - Record run conditions